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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,414	07/08/2004	Mark R. Bilak	BUR920010045US2	4413

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MCGUIRE WOODS LLP
1750 TYSONS BLVD.
SUITE 1800
MCLEAN, VA 22102-4215

EXAMINER
CHEN, ALAN S

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,414	BILAK ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

05/26/06

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/08/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: pages in the specification should be numbered.

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-12 are rejected on the ground of nonstatutory double patenting over claim claims 1-11 of U.S. Patent No. 6,877,048 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming

common subject matter, as follows: both claim an apparatus and method that dynamically allocates buffer memory between an inbound and outbound buffer based on need, block sizes in the buffer being smaller than the maximum frame size, and the inbound and outbound memories having a dedicated processor to control transfer and buffer memory allocation. While linked lists and processor threads are claimed in the patent, they are well known to one of ordinary skill in the art, where link lists are used to associate order to the buffer elements and processor threads are units of work associated with processors.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1,2 and 7-12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pat. No. 6,219,728 to Yin.

6. Per claim 1, Yin discloses an apparatus for processing packets *(Fig. 2, switch with multiple input and output ports; Column 3, lines 40-53 detail network traffic in the form of data cells equivalent to data packets)* comprising: an inbound memory for receiving data packets *(Figs. 5-7 shows separate buffers $Q_1 \ldots Q_n$, the buffers from a pool of buffers, element 102, the buffers being assigned as inbound buffer memory; Fig. 1 shows the input buffers and output buffers being consolidated into to the switch shared memory, where $Q_1 \ldots Q_n$, represent the input and output buffers)*; an outbound memory for transmitting data packets *(Fig. 1, element 14 is represented by a subset of Fig. 1, elements $Q_1 \ldots Q_n$)*; and circuitry *(Fig. 8B, processor)* capable of dynamically allocating memory from the inbound memory for use by the outbound memory or vice versa *(Figs. 5-7; Column 5, lines 39+ expressly disclose inactive queues have their buffer space dynamically reallocated so active queues can have a larger buffer threshold)*.

7. Per claims 7 and 10, claim 1 is substantially similar and therefore the rejection is applied accordingly to these claims.

8. Per claim 2, Yin discloses claim 1, wherein the outbound and inbound memories have a size that is smaller than the maximum frame size of the data packet to be processed *(Fig. 4; Column 4, lines 10-20, the frame size is shown in element 108, the frame has a plurality of ATM cells 109, the cells are what get stored in each element of the buffers, therefore the memory size per element is less than the frame size)*.

9. Per claims 8,9 and 11,12, Yin discloses claims 7 and 11, wherein the step of dynamically allocating includes the steps of determining that the inbound and/or

outbound memory buffer requires additional memory and dynamically allocating it more memory from inactive outbound and/or inbound buffers *(Column 5, lines 55+)*.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yin in view of US Pat. No. 5,748,629 to Caldara et al. (Caldara).

Yin discloses claim 1 and a processor controlling/processing cells/packets *(Figs. 8A and 8B)*. Yin further discloses the processor determining the amount of memory to allocate to each buffer *(Fig. 8B, element 132 and Fig. 8C)*.

Yin does not disclose expressly two distinct processors, one to handle inbound memory tasks and the other to handle outbound memory tasks and communications between the two processors for buffer allocation.

Caldara discloses a switch having a plurality of input ports and output ports where the each of the ports has its own processing and buffering logic for inbound and outbound packets *(Fig. 1, elements 14 and 16 are the inbound and outbound processors. Elements 41 and 61 are the buffer memories)*. Caldara further discloses having a bandwidth arbiter to determine how much bandwidth is allocated to each port, which is directly related to how fast the buffers fill *(Fig. 1, element 11)*.

Yin and Caldara are analogous art because they are from similar problem solving area particular to ATM switching. In fact, Yin directly shows the same switching structure as Caldara *(Fig. 1, input and output buffers are outside the switch just like Caldara)*.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have separate processors for the input and output ports of the switch and the processors handling buffer allocation between the input and output ports.

The suggestion/motivation for doing so is that significant processing is required at the I/O ports in analyzing the incoming and outgoing data cells, particularly if the switch is used in an environment with high levels of data traffic (Column 2, lines 55-67 of Caldara). Separate processors will distribute the processing load by assigning specific tasks to each processor such as inbound or outbound processing tasks.

Therefore, it would have been obvious to combine Yin with Caldara for the benefit increasing the capability and performance of the switch.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patents and patent related publications are cited in the Notice of References Cited (Form PTO-892) attached to this action to further show the state of the art with respect to dynamic allocation of buffer resources.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ASC
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